Description

The SMDAxxLC and SMDAxxLCC Series are low capacitance multi-line transient voltage suppressor arrays that provides board level protection for standard TTL and MOS bus line applications against the damaging effects of ESD, tertiary lightning and switching transients.

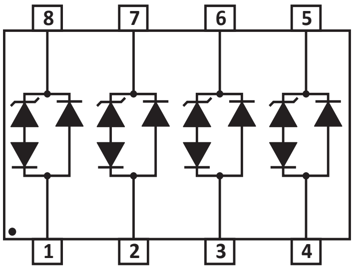
The SMDAxxLC/LCC Series has a peak pulse power rating of 300 W for an 8/20μs waveshape. This device series ,meets the IEC 61000-4-2, IEC61000-4-4 and IEC 61000-4-5 requirements.

Mechanical Characteristics

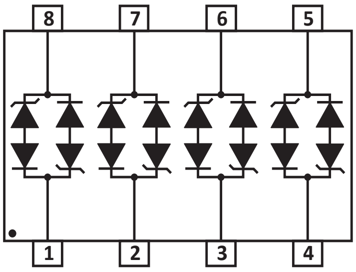
- Molded JEDEC SO-8 Package
- Approximate Weight: 70 milligrams
- Lead -Free Pure -Tin Plating (Annealed)
- Solder Reflow Temperature:
  Pure -Tin -Sn, 100: 260-270°C
- 12mm Tape and Reel Per EIA Standard 481
- Flammability Rating UL 94V-0

Dimensions and Pin Configuration

Unidirectional



Bidirectional



Device Marking Code

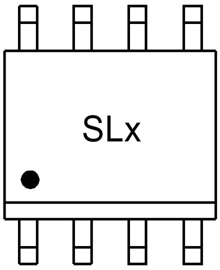
Features

- Compatible with IEC 61000-4-2 (ESD): Air -15KV, Contact -8KV
- Compatible with IEC 61000-4-4 (EFT): 40A -5/50ns
- Compatible with IEC 61000-4-5 (Surge): 12A, 8/20μs - Level 1 (Line - Gnd) & Level 2 (Line - Line)
- 500W Peak Pulse Power per line (tp=8/20μs)
- Unidirectional and Bidirectional Configurations
- Available in Multiple Voltages Ranging from 3V to 24V
- Protects up to Four Lines
- Low Capacitance: 1pF
- RoHS Compliant
- REACH Compliant

Applications

- Computer Interface Protection
- Ethernet – 10/100/1000 Base T
- Test and Measurement Equipment
- Industrial Control -Low Voltage Sensors

Marking Information



Dot denotes Pin1

Ordering Information

Part Number	Marking	Packaging	Reel Size
SMDAxxLC/LCC	SLx	2500/Tape & Reel	13 inch

Absolute Maximum Ratings (T_A=25°C unless otherwise specified)

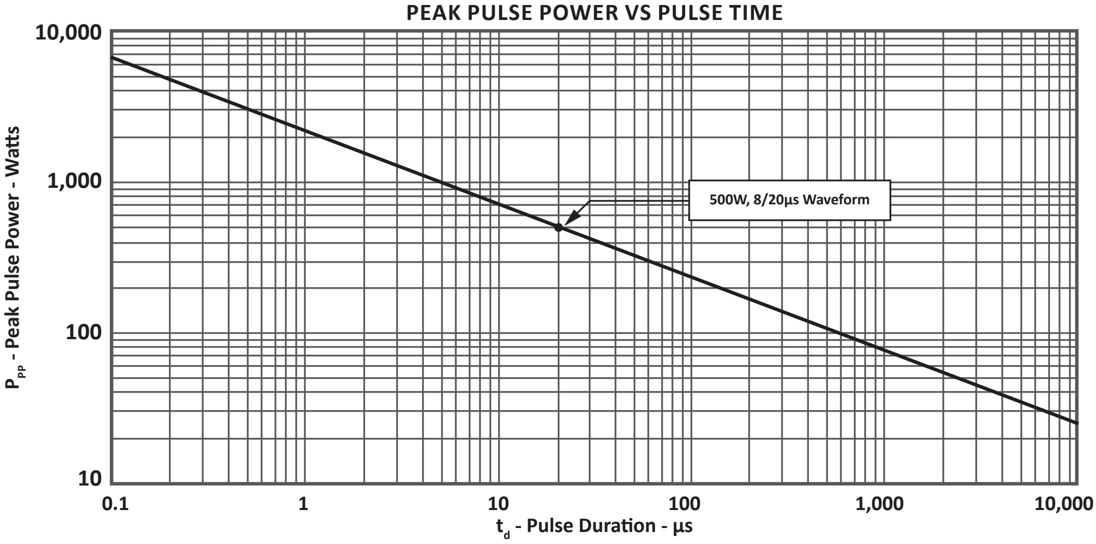
Parameter	**Symbol**	**Value**	**Unit**
Peak Pulse Power(8/20μs)	Ppk	300	W
Forward Voltage(50mA/300μs)	V_F	1.5	V
Operating Temperature Range	T_J	−55 to +150	°C
Storage Temperature Range	Tstg	−55 to +150	°C

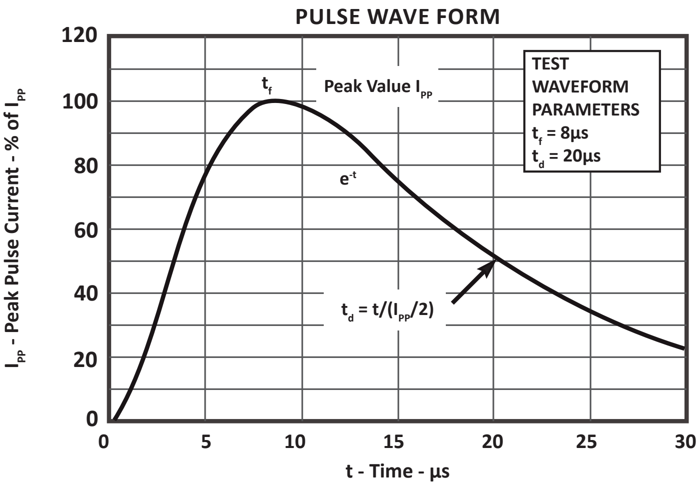
Electrical Characteristics (T_A=25°C unless otherwise specified)

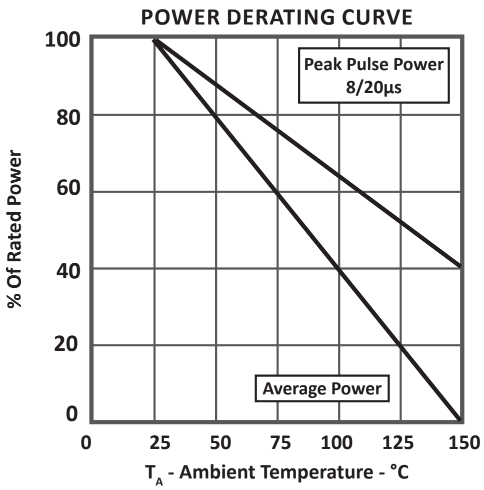
Part Number（Note1）	**Device Marking**	**Rated Stand-off Voltage V_{WM}(V)**	**Minimum Breakdown Voltage @1mA V_{BR}(V)**	**Maximum Clamping Voltage @I_P=1A V_C(V)**	**Maximum Clamping Voltage @8/20μs V_C@I_{PP}(V)**	**Maximum Leakage Current @V_{WM} IR(μA)**	**Maximum Capacitance @0V,1MHz C_J(pF)**
SMDA03LC	SLA	3.3	4.5	7.0	14.0V@18.0A	0.1	1
SMDA03LCC	SLB	3.3	4.5	7.0	14.0V@18.0A	0.1	1
SMDA05LC	SLC	5.0	6.0	9.8	16.0V@16.0A	0.1	1
SMDA05LCC	SLD	5.0	6.0	9.8	16.0V@16.0A	0.1	1
SMDA08LC	SLE	8.0	8.5	13.4	19.0V@13.0A	0.1	1
SMDA08LCC	SLF	8.0	8.5	13.4	19.0V@13.0A	0.1	1
SMDA12LC	SLG	12.0	13.3	19.0	25.0V@10.0A	0.1	1
SMDA12LCC	SLH	12.0	13.3	19.0	25.0V@10.0A	0.1	1
SMDA15LC	SLJ	15.0	16.7	24.0	31.0V@8.0A	0.1	1
SMDA15LCC	SLK	15.0	16.7	24.0	31.0V@8.0A	0.1	1
SMDA24LC	SLL	24.0	26.7	43.0	71.0V@3.5A	0.1	1
SMDA24LCC	SLM	24.0	26.7	43.0	71.0V@3.5A	0.1	1

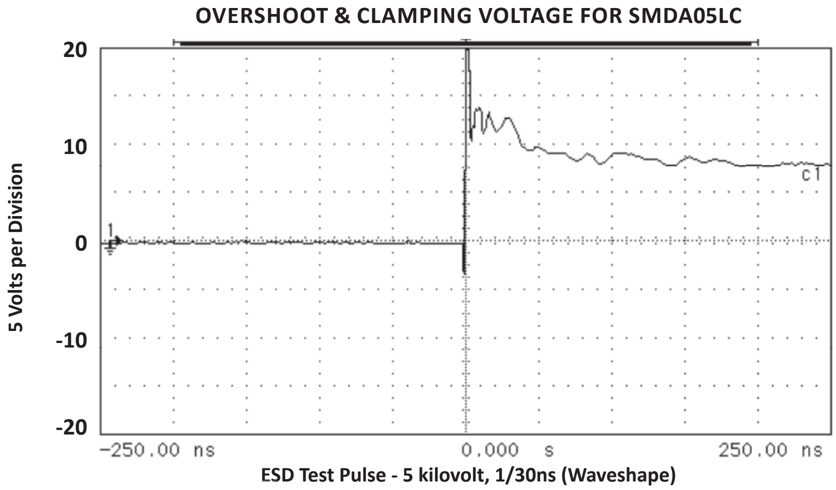
Notes
1.Part numbers with a “C” suffix are bidirectional devices,i.e.,SMDA03LCC.

Typical Characteristics

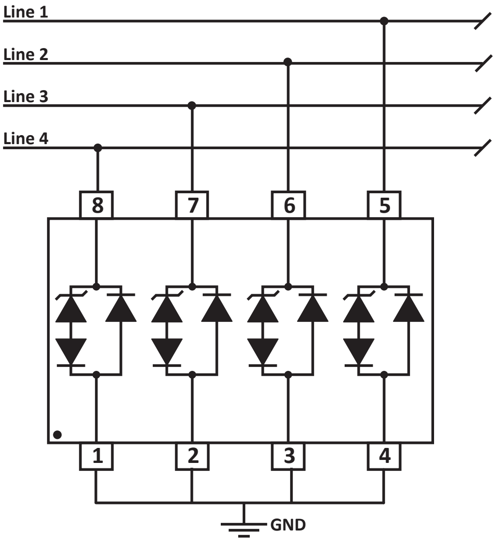








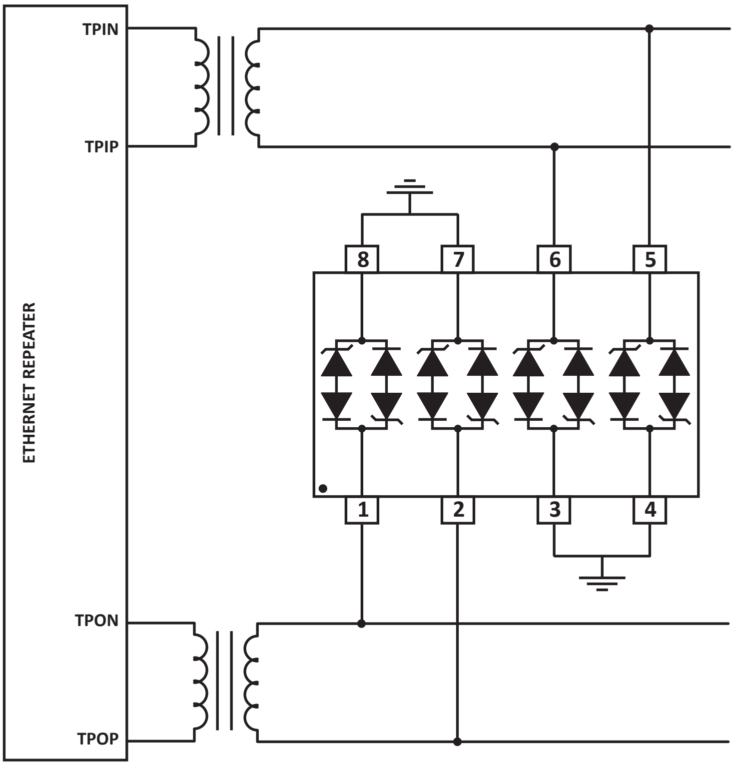
Application Information



UNIDIRECTIONAL COMMON-MODE PROTECTION

Circuit connectivity is as follows:

- Line 1 connected to Pin 5.
- Line 2 connected to Pin 6.
- Line 3 connected to Pin 7.
- Line 4 connected to Pin 8.
- Pins 1 - 4 connected to ground.



BIDIRECTIONAL COMMON-MODE ETHERNET PROTECTION

Circuit connectivity is as follow:

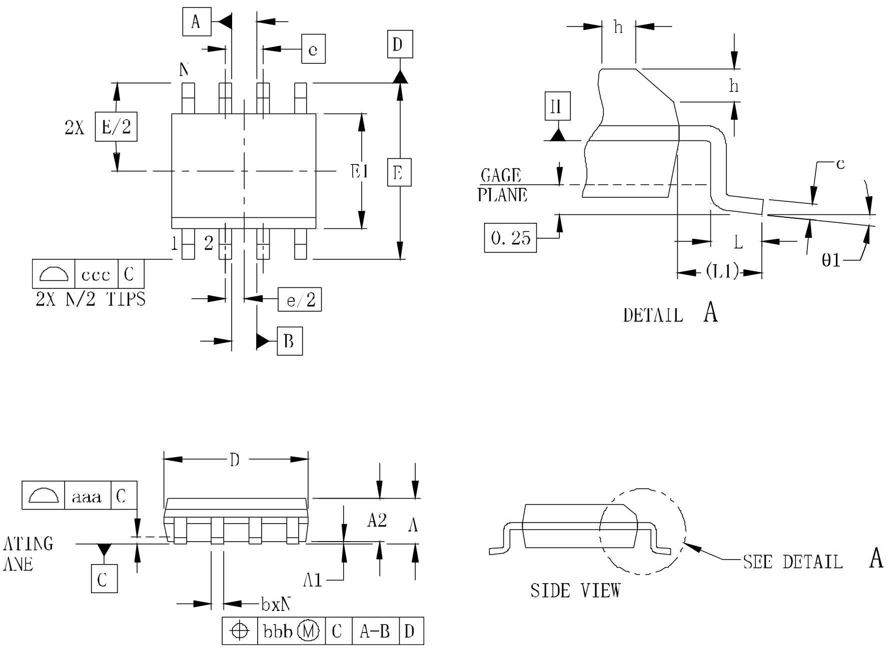
- TPIN connected to Pin 5.
- TPIP connected to Pin 6.
- TPON connected to Pin 1.
- TPOP connected to Pin 2.
- Pins 3, 4, 7 and 8 connected to ground.

CIRCUIT BOARD RECOMMENDATIONS

Circuit board layout is critical for electromagnetic compatibility protection. The following guidelines are recommended:

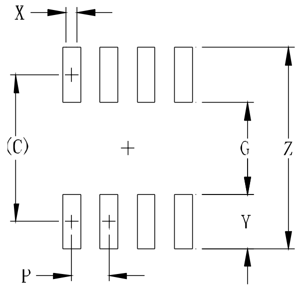
- The protection device should be placed near the input terminals or connectors, the device will divert the transient current immediately before it can be coupled into the nearby traces.
- The path length between the TVS device and the protected line should be minimized.
- All conductive loops including power and ground loops should be minimized.
- The transient current return path to ground should be kept as short as possible to reduce parasitic inductance.
- Ground planes should be used whenever possible. For multilayer PCBs, use ground vias.

SO-8 Package Outline Drawing



SYM	DIMENSIONS					
	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.35		1.75	0.053		0.069
A1	0.10		0.25	0.004		0.010
A2	1.25		1.65	0.049		0.065
b	0.31		0.51	0.012		0.020
c	0.17		0.25	0.007		0.010
D	4.80	4.90	5.00	0.189	0.193	0.197
E1	3.80	3.90	4.00	0.150	0.154	0.157
E	6.00 BSC			0.236 BSC		
e	1.27 BSC			0.050 BSC		
h	0.25		0.50	0.010		0.020
L	0.40	0.72	1.04	0.016	0.028	0.041
L1	(1.04)			(0.041)		
N	8			8		
θ1	0°		8°	0°		8°
aaa	0.10			0.004		
bbb	0.25			0.010		
ccc	0.20			0.008		

Suggested Land Pattern



SYM	DIMENSIONS	
	MILLIMETERS	INCHES
C	(5.20)	0.205
G	3.00	0.118
P	1.27	0.050
X	0.60	0.024
Y	2.20	0.087
Z	7.40	0.291

Contact Information

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